Notice of Allowability	Application No.	Applicant(s)	
	09/874,027	DANCEA, IOAN	
	Examiner	Art Unit	
	Fred Ferris	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *22 September 2005*.

2. ☒ The allowed claim(s) is/are *2-9 and 12-15*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

AU 2128

DETAILED ACTION

1. This Office action is responsive to applicant's amendment filed on 22 September 2005. Applicant's amendment has cancelled claims 1, 10, and 11. Claims 2-9 and 12-15 are currently pending in this application.

Response to Arguments

2. Applicant's arguments filed 22 September 2005 have been fully considered and found to be persuasive. The previous rejections and objections have now been withdrawn in view of applicant's amendment to the claims, specification, and arguments submitted 22 September 2005. Accordingly, the case is now in condition for allowance.

EXAMINER'S AMENDMENT

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

This examiners amendment has been presented in order to clarify the amendment to the specification and Figures as presented on page 1, paragraph 2 to page 3 paragraph 2 of applicant's submission dated 22 September 2005 in the interest of accurate publication and customer assistance in this pro se application. This amendment is in addition to the changes of applicant's preliminary amendment filed 6 June 2002.

Amend the specification as follows:

Delete *the text beginning on page 19, line 9 to page 20, line 7 and* ***insert*** *the text beginning on page 2, line 7 to page 3, line 3 of applicants amendment dated 22 September 2005. (This corresponds to paragraphs 0101 to 0108 of applicants Patent Application Publication US 2002/0173938 A1.) The text beginning on page 19, line 9 should now read "****A second embodiment of the proposed VLSI device....****".*

Delete *the text on page 6, lines 20 and 21 and* ***insert*** *the following text:*

*"****Figure 10 shows the application of mask words and product words to associated inputs to provide output of the considered independent equation.***

Figure 11 shows the second embodiment of the VLSI device implementing only the independent equation.

Figure 12 shows the independent equation using the modified cell with mask word register and product word register connected to the associated combinational part.*"*

(This corresponds to paragraph 0031 of applicants Patent Application Publication US 2002/0173938 A1.)

Amend the drawings as follows:

Delete *Figures A, B, and C from applicant's replacement drawing sheets (pages 15-17) submitted 20 April 2005. Only Figures 1-12 (pages 1-14) should remain.* ***Delete*** *the phrase "Replacement Sheet" from the top of Figures 1-12.*

Allowable Subject Matter

4. *Claims 2-9 and 12-15 have now been allowed over the prior art of record.*

The following is an examiner's statement of reasons for allowance:

Applicants are disclosing semiconductor device circuit technique for implementing a combinatorial circuit with functions expressed in sum-of-product equations implemented using a resister storing input variables, multiple cells, a product term cell, and summing circuit receiving product term values. This has been disclosed in the prior art of record.

While these elements are individually disclosed in the prior art, the prior art of record does not meet the conditions as suggested in MPEP section 2132, namely:

"The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, i.e., identity of terminology is not required. In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)."

Per independent claim 12: In particular, the prior art of record does not disclose the specific arrangement of elements consisting of modified cell C(k) for determining logical value of a product term for an independent equation and a single OR gate associated with the modified cell receiving product terms p(k) to provide a single independent equation output, where the modified cell includes a storage area formed by two m-bit registers for storing mask word and product word, a first logic level comprising

AND gates receiving mask word intermediate result forming a product term, a second logic level comprising XNOR gates receiving product word intermediate product term, and a third logic level comprising one AND gate receiving intermediate result to produce a logical value of the product term as now recited in the independent claim 12. (See: Figs. 2-4, 7-11, for example)

Per independent claim 2: In addition to the reasoning cited above, the "means for" language of claim 2 is given deference in view of In re Donaldson and interpreted in view of 35 U.S.C. § 112 paragraph 6. The "means for" language and the limitations related thereto is therefore interpreted within the scope of enablement as provided within the relative embodiment provided within applicant's specification as follows:

- *first logic "means for" receiving m mask word inputs to produce intermediate result: page 8, line 2 to page 15, line 20, Figs. 2A-4, 6-8*
- *second logic "means for" comparing product term product term producing second intermediate result: page 8, line 2 to page 15, line 20, Figs. 2A-4, 6-8*
- *third logic "means for" receiving second intermediate result producing product term: page 8, line 2 to page 15, line 20, page 16, line 25 to page 20, line 7, Figs. 2A-4, 8, 11*

- *forth logic "means for" transferring function word outputs: page 8, line 2 to page 15, line 20, page 16, line 25 to page 20, line 7, Figs. 2A-4*

The closest prior art uncovered during examination teaches certain limitations of the claimed invention as follows:

- U.S. Patent 6,034,546 issued to Jones: teaches a VLSI circuit technique for implementing a combinatorial circuit inclusive of functions expressed in sum-of-product equations, a register storing input variables, multiple cells, and summing circuit receiving product term values but does not disclose the specific arrangement of elements consisting of modified cell determining product term for an independent equation, single OR gate associated with the modified cell including a storage area formed by two m-bit registers for storing mask word and product word, or the specific first to forth logic levels as required by independent claims 2 and 12.

- U.S. Patent 6,212,670 issued to Kaviani: discloses the use a product term cell for determining the logical value of the product term equations from the input but again does not disclose the specific arrangement of elements consisting of modified cell determining product term for an independent equation, single OR gate associated with the modified cell including a storage area formed by two m-bit registers for storing mask word and product word, or the specific first to forth logic levels as required by independent claims 2 and 12.

The features noted above relating to the specific arrangement of combinational circuit elements and the "means for" language now recited in the independent claims 2 and 12 renders the claimed invention non-obvious over the prior art of record.

Dependent claims 3-9, and 13-15 are deemed allowable as being dependent from independent claims 2 and 12 respectively.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 571-272-3778 and whose normal working hours are 8:30am to 5:00pm Monday to Friday. Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 571-272-3700. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached at 571-272-2279. The Official Fax Number is: (703) 872-9306

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